LRE TRAINING PROGRAM

{Audio Cassette w/Diagrams}

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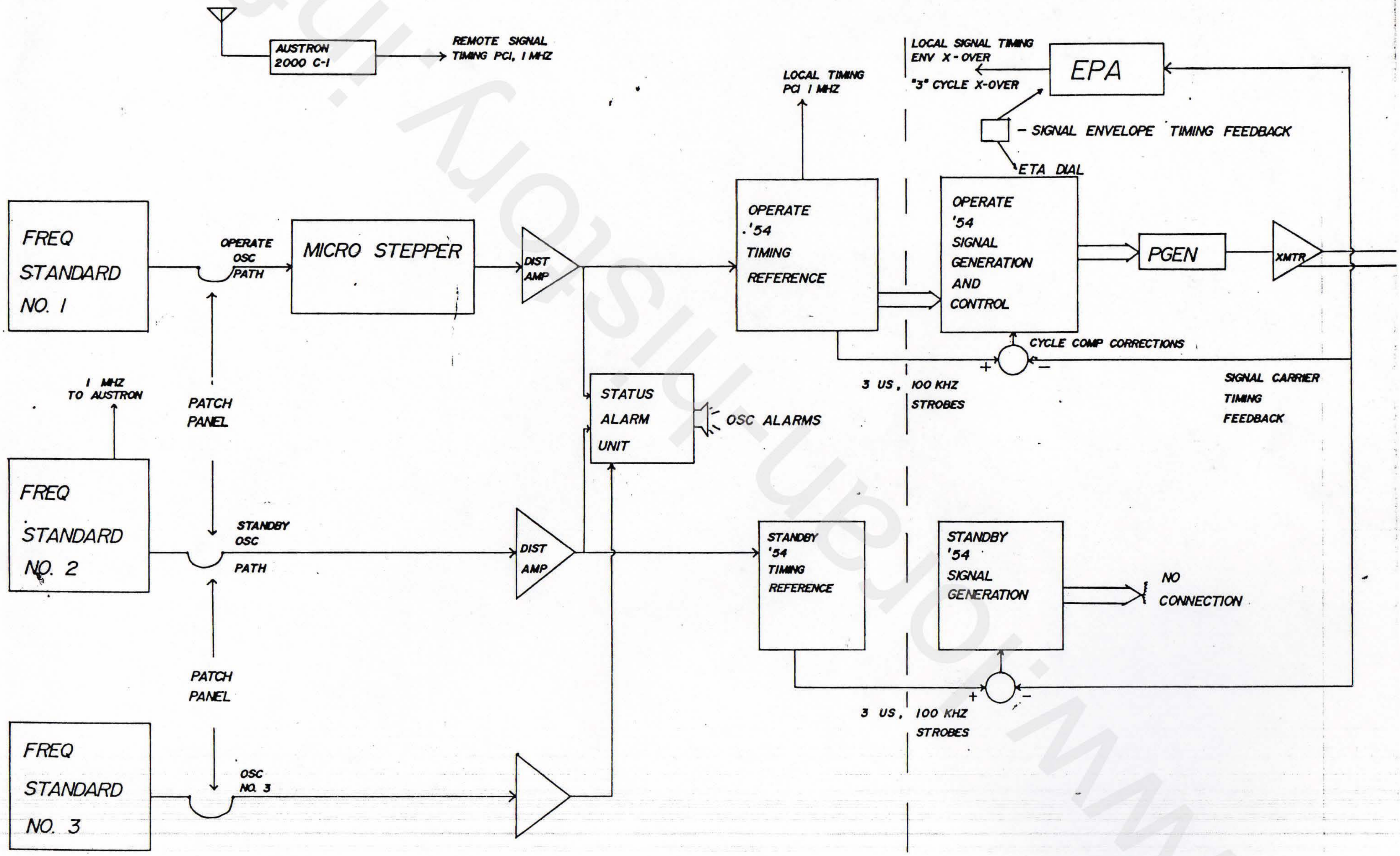
NONE NE	INSTRUCTIONS FOR CASUALTY DRILLS AS DONE AT DANA	NONE NONE	P15-29



LORAN 'MING ·RAN SIGNAL GENER ION

FIGURE 1-1

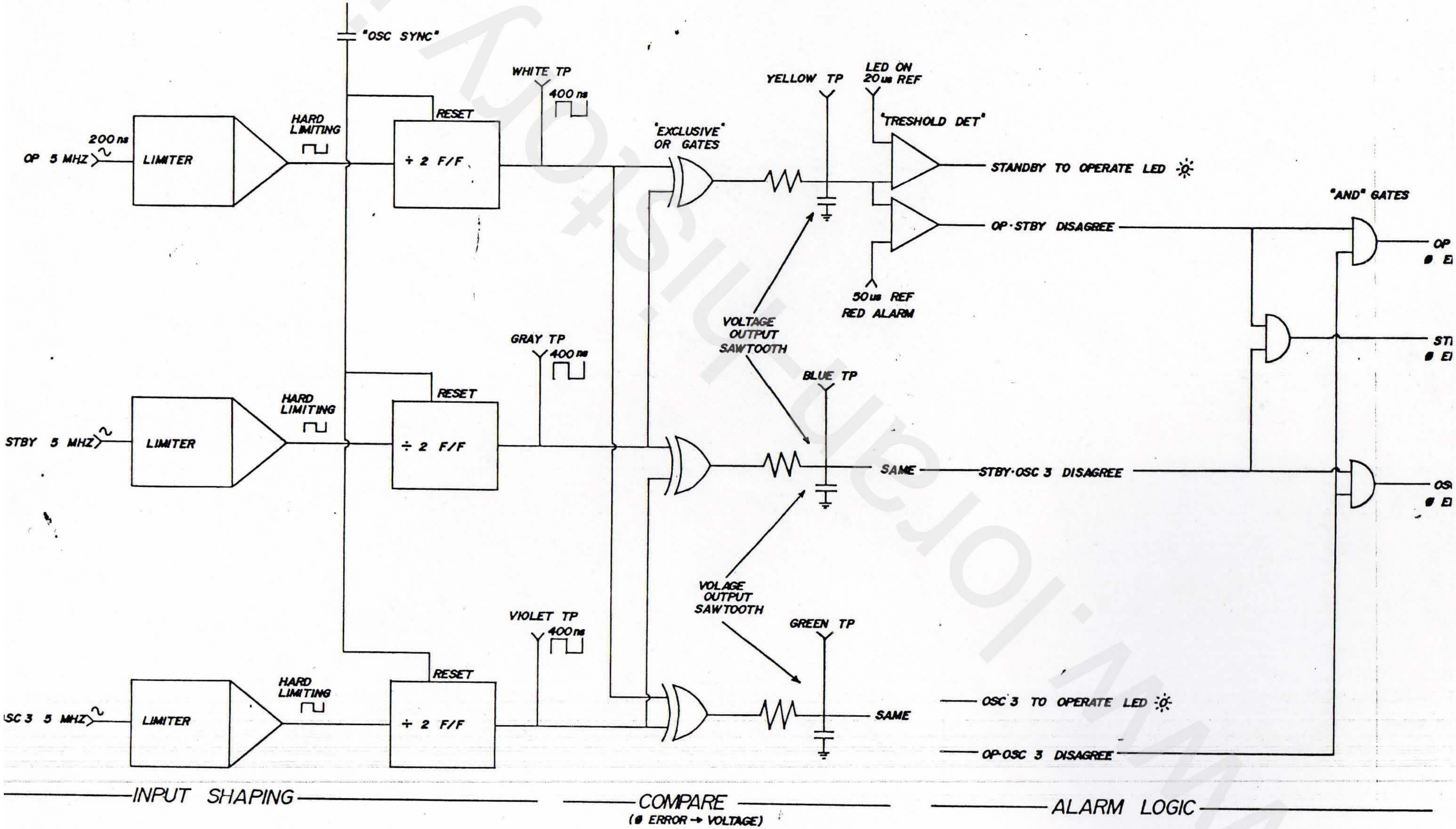
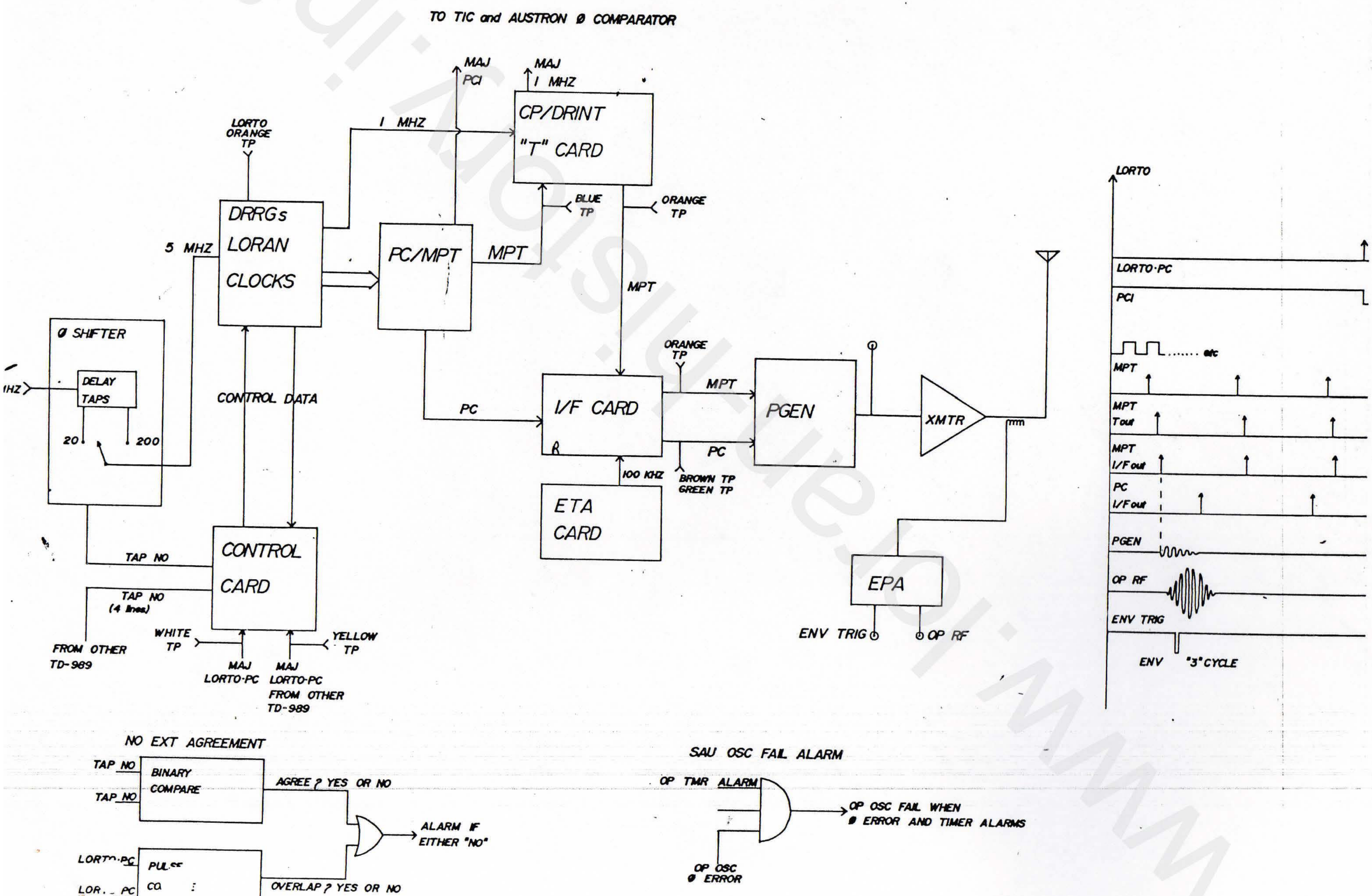

"OSC SYNC"
OP 5 MHZ
200 ns
STBY 5 MHZ
SC 3 5 MHZ
LIMITER
LIMITER
LIMITER
HARD LIMITING
HARD LIMITING
HARD LIMITING
RESET
RESET
RESET
÷ 2 F/F
÷ 2 F/F
÷ 2 F/F
WHITE TP
400 ns
GRAY TP
400 ns
VIOLET TP
400 ns
"EXCLUSIVE" OR GATES
VOLTAGE OUTPUT SAWTOOTH
VOLAGE OUTPUT SAWTOOTH
YELLOW TP
BLUE TP
GREEN TP
LED ON 20 us REF
"TRESHOLD DET"
50 us REF
RED ALARM
STANDBY TO OPERATE LED
OP·STBY DISAGREE
SAME
STBY·OSC 3 DISAGREE
SAME
OSC 3 TO OPERATE LED
OP·OSC 3 DISAGREE
"AND" GATES
OP
ST
OS
INPUT SHAPING
COMPARE
(Ø ERROR → VOLTAGE)
ALARM LOGIC

FIGURE 1-2



TO TIC and AUSTRON Ø COMPARATOR
MAJ PCI
MAJ 1 MHZ
CP/DRINT "T" CARD
1 MHZ
LORTO ORANGE TP
DRRGs LORAN CLOCKS
5 MHZ
PC/MPT
MPT
BLUE TP
ORANGE TP
Ø SHIFTER
DELAY TAPS
20
200
CONTROL DATA
PC
I/F CARD
ORANGE TP
MPT
PC
PGEN
XMTR
100 KHZ
BROWN TP
GREEN TP
ETA CARD
CONTROL CARD
TAP NO
TAP NO (4 lines)
FROM OTHER TD-989
WHITE TP
MAJ LORTO-PC
MAJ LORTO-PC FROM OTHER TD-989
YELLOW TP
EPA
ENV TRIG
OP RF
LORTO
LORTO·PC
PCI
etc
MPT
MPT Tout
MPT I/F out
PC I/F out
PGEN
OP RF
ENV TRIG
ENV "3" CYCLE
NO EXT AGREEMENT
TAP NO
TAP NO
BINARY COMPARE
AGREE ? YES OR NO
ALARM IF EITHER "NO"
OVERLAP ? YES OR NO
SAU OSC FAIL ALARM
OP TMR ALARM
OP OSC FAIL WHEN Ø ERROR AND TIMER ALARMS
OP OSC Ø ERROR

FIGURE 1-3

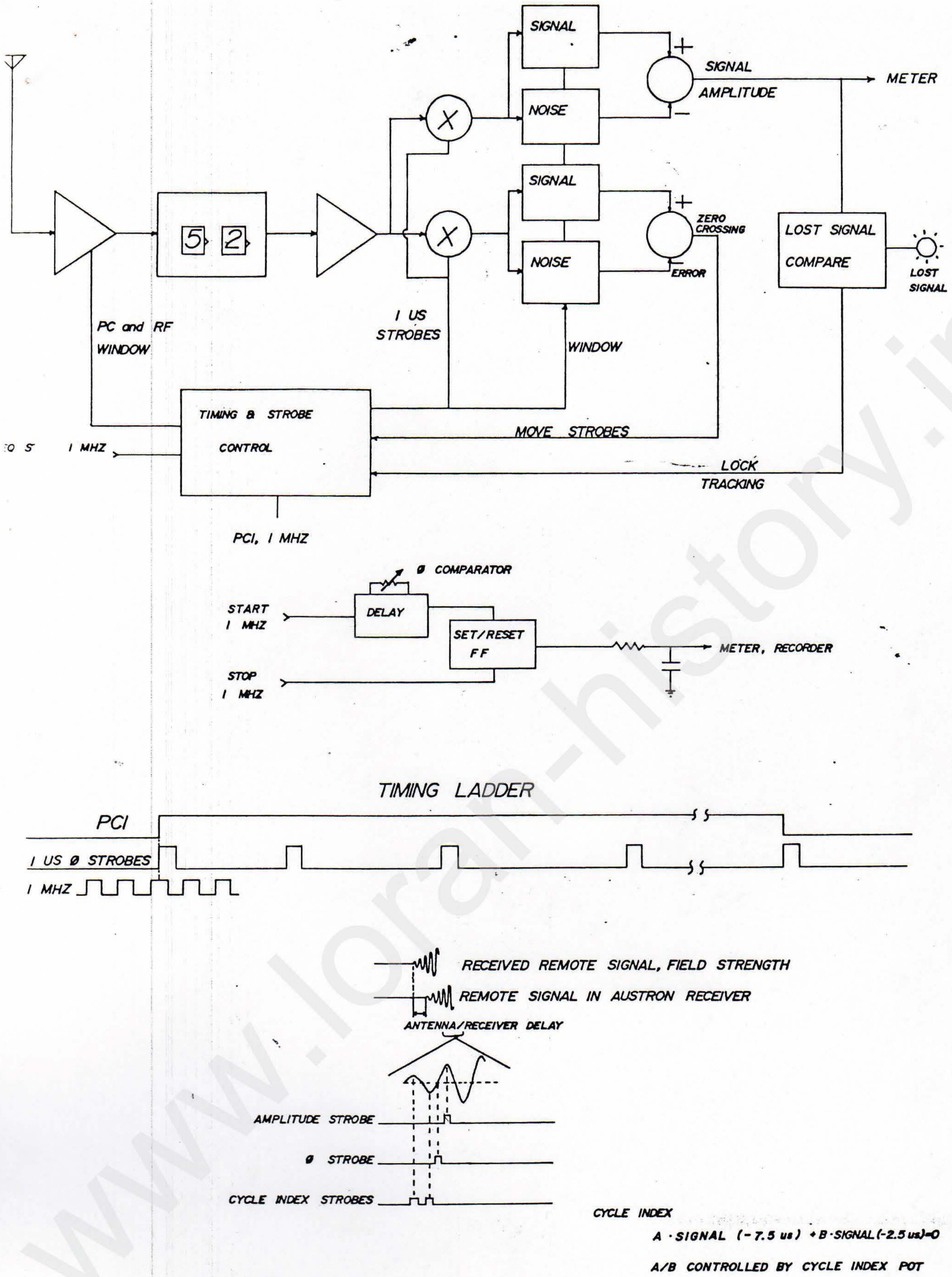


FIGURE 1-4

AUSTRON RECEIVER FUNCTIONAL DIAGRAM and TIMING RELATIONS

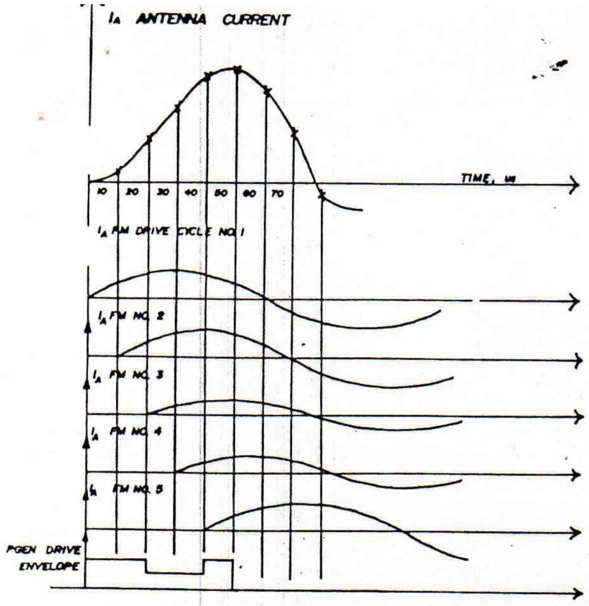


FIGURE 4-4

TYPICAL FPN-39,42 ANTENNA RESPONSE

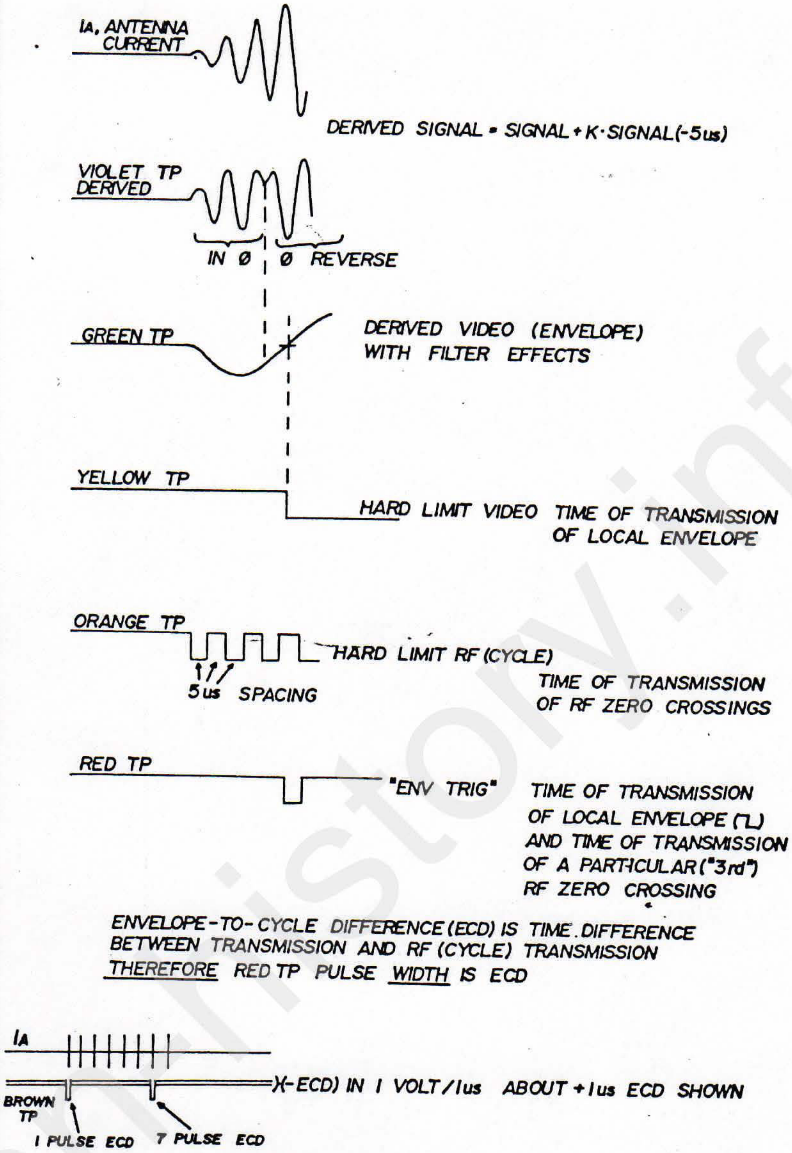
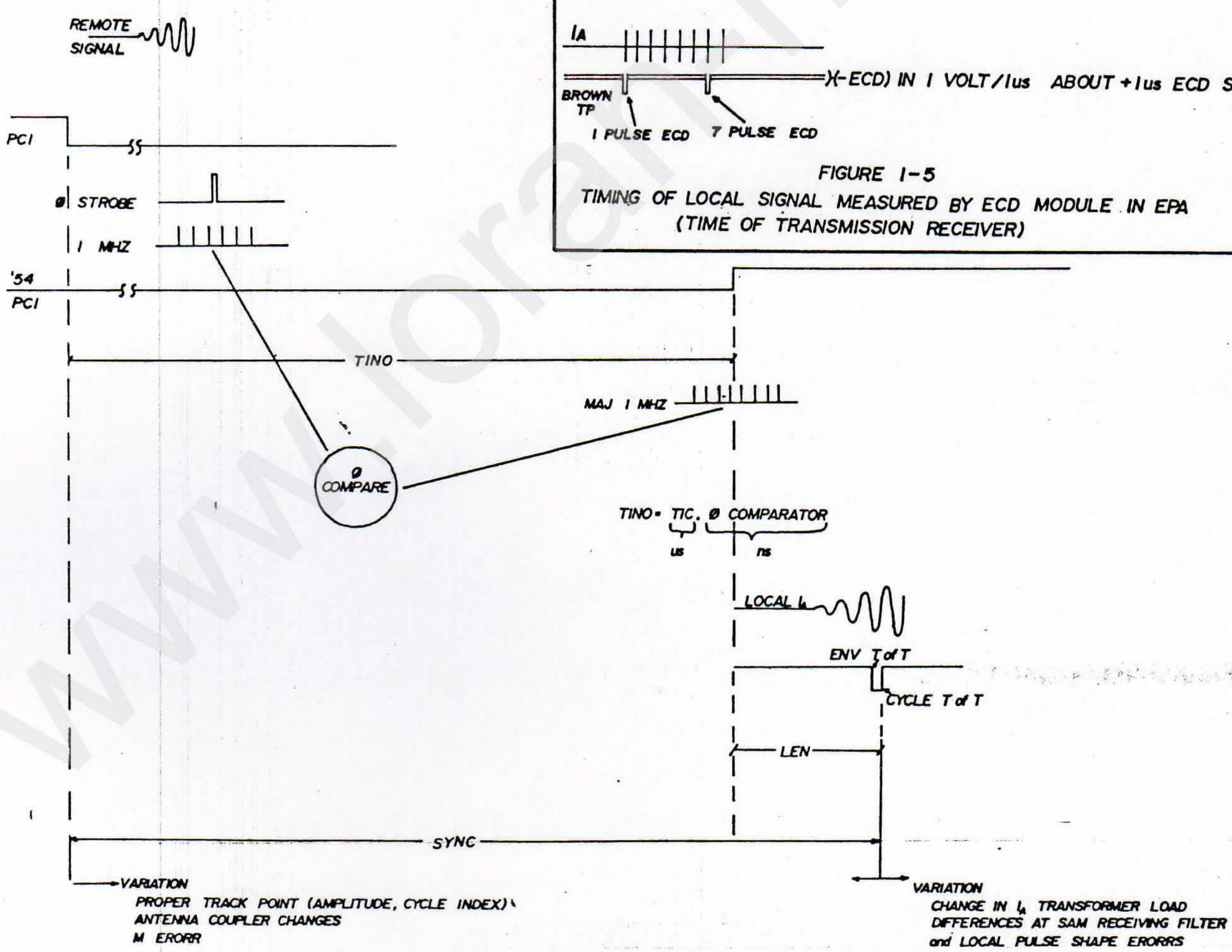


FIGURE 1-5

TIMING OF LOCAL SIGNAL MEASURED BY ECD MODULE IN EPA (TIME OF TRANSMISSION RECEIVER)



NOTE 1: AT LORSTA DANA, OPER 5MHZ IS FED TO THE RECORDERS FROM DIST AMP BY CH 1 TO RECORDER NO.1 and CH 3 TO RECORDER NO.2

NOTE 2: DISCONNECTED AT DANA LORSTA.

NOTE 3: DOES NOT GO THROUGH DIST AMP AT LORSTA DANA.

NOTE 4: AS SHOWN HOOKED UP IN TECH MANUAL.

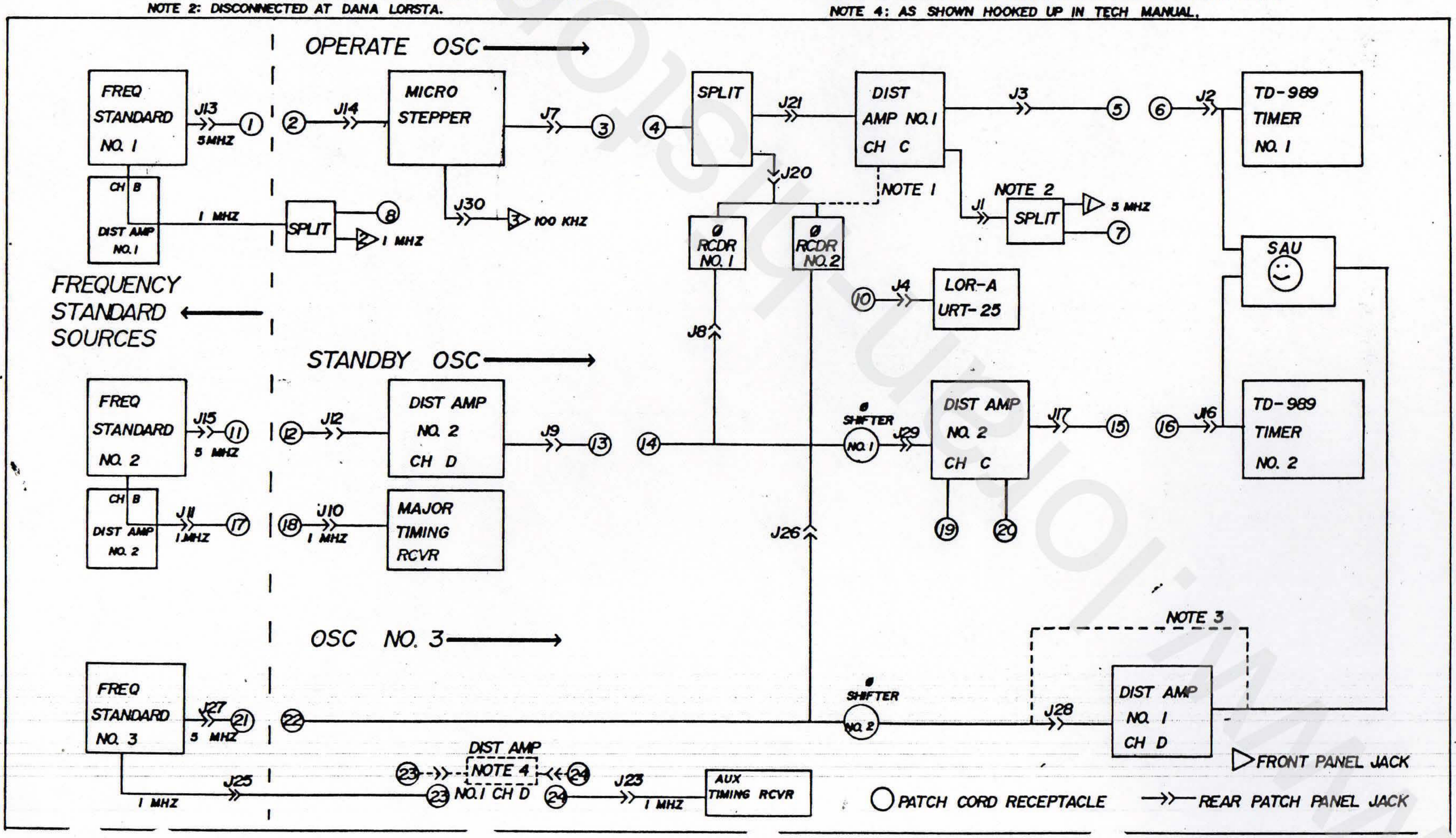
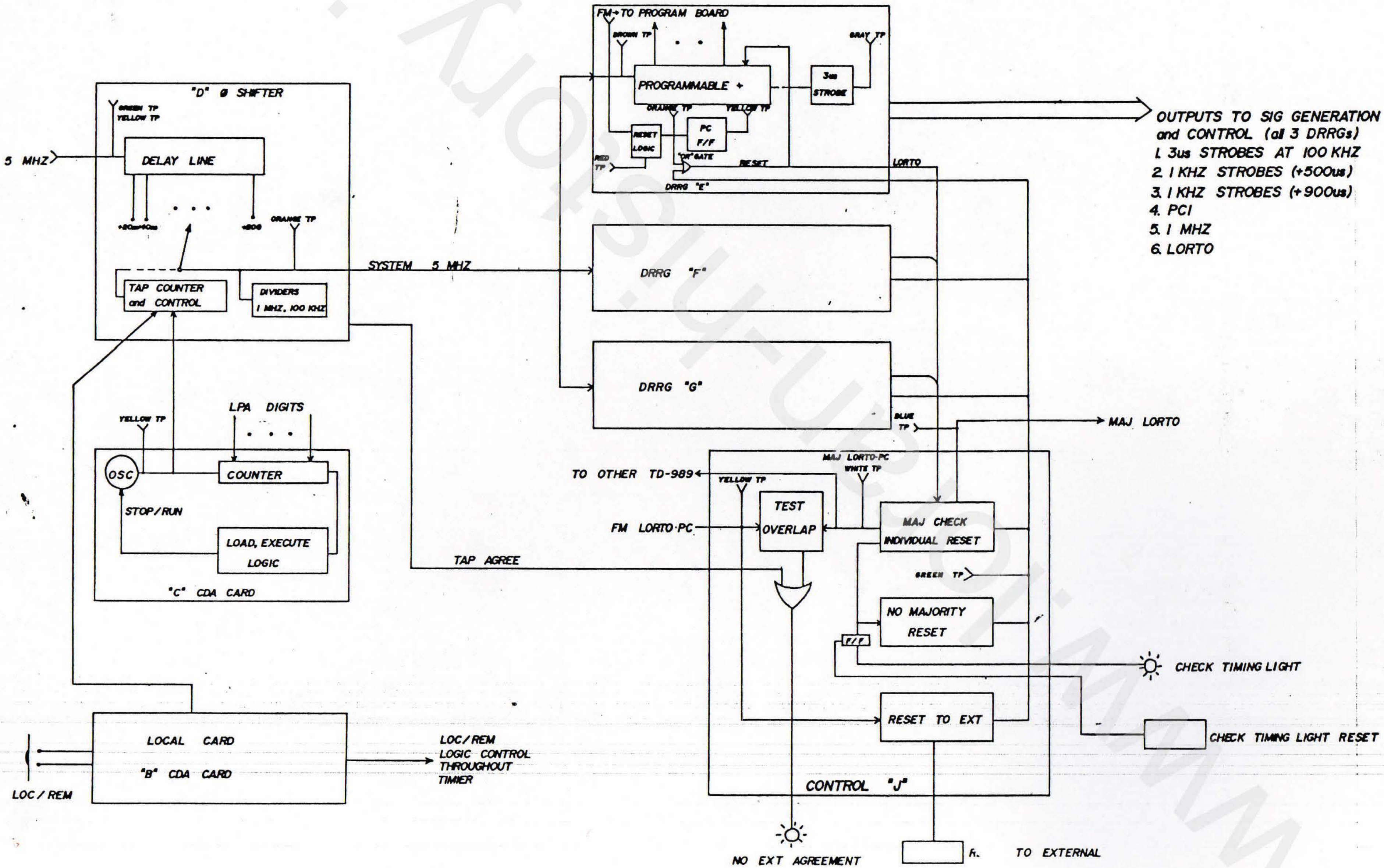


FIGURE 3-1

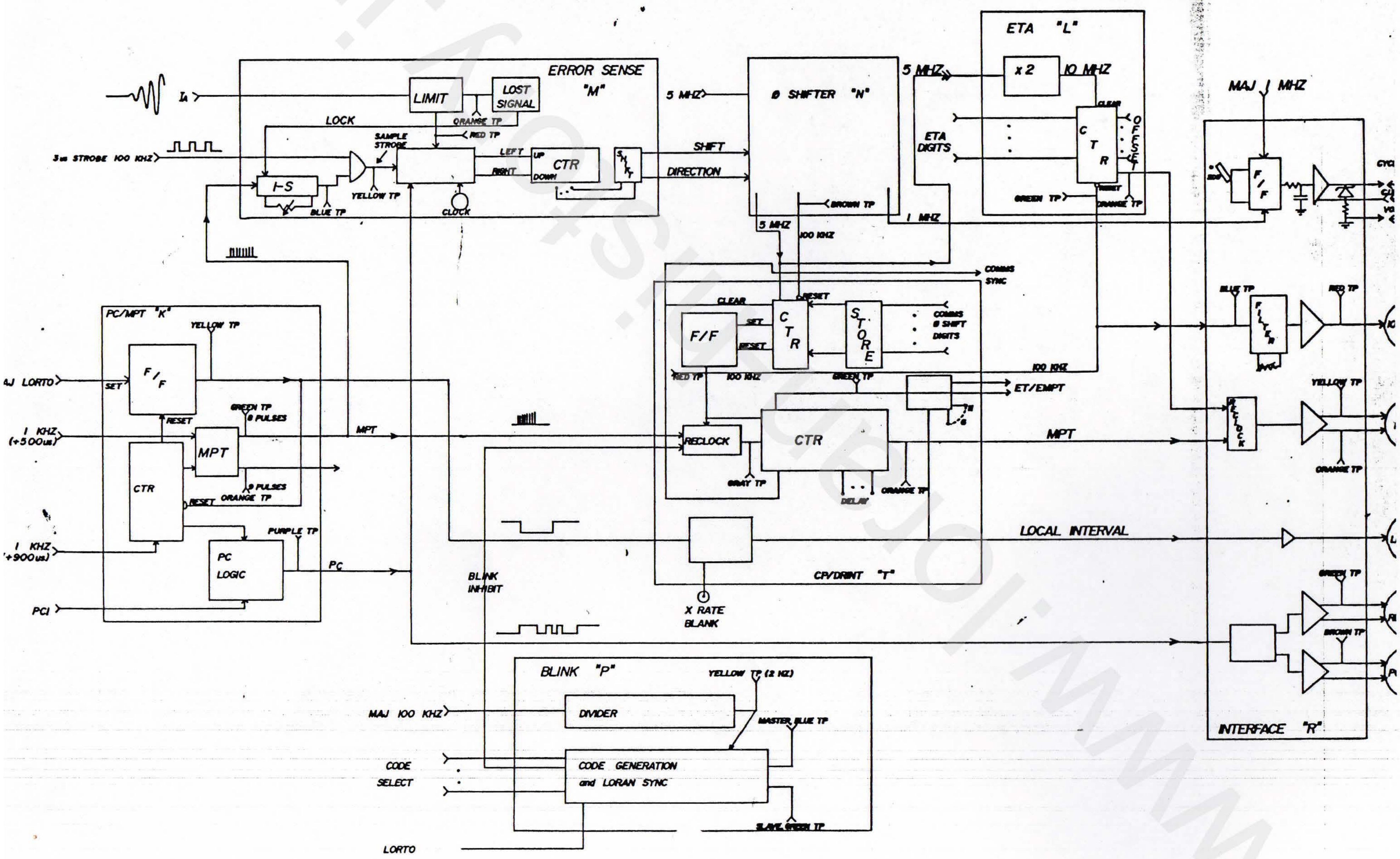
FREQUENCY STANDARD RACK PANEL



"D" Ø SHIFTER
GREEN TP
YELLOW TP
5 MHZ
DELAY LINE
ORANGE TP
TAP COUNTER and CONTROL
DIVIDERS 1 MHZ, 100 KHZ
SYSTEM 5 MHZ
YELLOW TP
LPA DIGITS
OSC
COUNTER
STOP/RUN
LOAD, EXECUTE LOGIC
"C" CDA CARD
LOCAL CARD
"B" CDA CARD
LOC/REM
LOC/REM LOGIC CONTROL THROUGHOUT TIMIER
TAP AGREE
FM→TO PROGRAM BOARD
BROWN TP
GRAY TP
PROGRAMMABLE ÷
3us STROBE
ORANGE TP
YELLOW TP
RESET LOGIC
PC F/F
"OR" GATE
RED TP
RESET
LORTO
DRRG "E"
DRRG "F"
DRRG "G"
OUTPUTS TO SIG GENERATION and CONTROL (all 3 DRRGs)
1. 3us STROBES AT 100 KHZ
2. 1 KHZ STROBES (+500us)
3. 1 KHZ STROBES (+900us)
4. PCI
5. 1 MHZ
6. LORTO
BLUE TP
MAJ LORTO
MAJ LORTO-PC WHITE TP
TO OTHER TD-989
YELLOW TP
FM LORTO·PC
TEST OVERLAP
MAJ CHECK INDIVIDUAL RESET
GREEN TP
NO MAJORITY RESET
F/F
CHECK TIMING LIGHT
RESET TO EXT
CHECK TIMING LIGHT RESET
CONTROL "J"
NO EXT AGREEMENT
TO EXTERNAL

FIGURE 3-2

P R



ERROR SENSE "M"
LIMIT
LOST SIGNAL
LOCK
SAMPLE STROBE
ORANGE TP
RED TP
LEFT
RIGHT
UP
DOWN
CTR
I-S
BLUE TP
YELLOW TP
CLOCK
3us STROBE 100 KHZ
SHIFT
DIRECTION
5 MHZ
Ø SHIFTER "N"
BROWN TP
100 KHZ
1 MHZ
ETA "L"
x 2
10 MHZ
ETA DIGITS
CLEAR
OFFSET
RESET
GREEN TP
ORANGE TP
MAJ 1 MHZ
COMMS SYNC
COMMS Ø SHIFT DIGITS
STORE
F/F
SET
RESET
RED TP
GREEN TP
ET/EMPT
RECLOCK
GRAY TP
DELAY
CP/DRINT "T"
X RATE BLANK
PC/MPT "K"
YELLOW TP
MAJ LORTO
1 KHZ (+500us)
1 KHZ (+900us)
PCI
MPT
8 PULSES
PC LOGIC
PURPLE TP
PC
BLINK INHIBIT
LOCAL INTERVAL
BLINK "P"
YELLOW TP (2 KHZ)
MAJ 100 KHZ
DIVIDER
MASTER BLUE TP
CODE SELECT
CODE GENERATION and LORAN SYNC
SLAVE GREEN TP
LORTO
INTERFACE "R"
BLUE TP
RED TP
FILTER
YELLOW TP
ORANGE TP
GREEN TP
BROWN TP

FIGURE 3-3

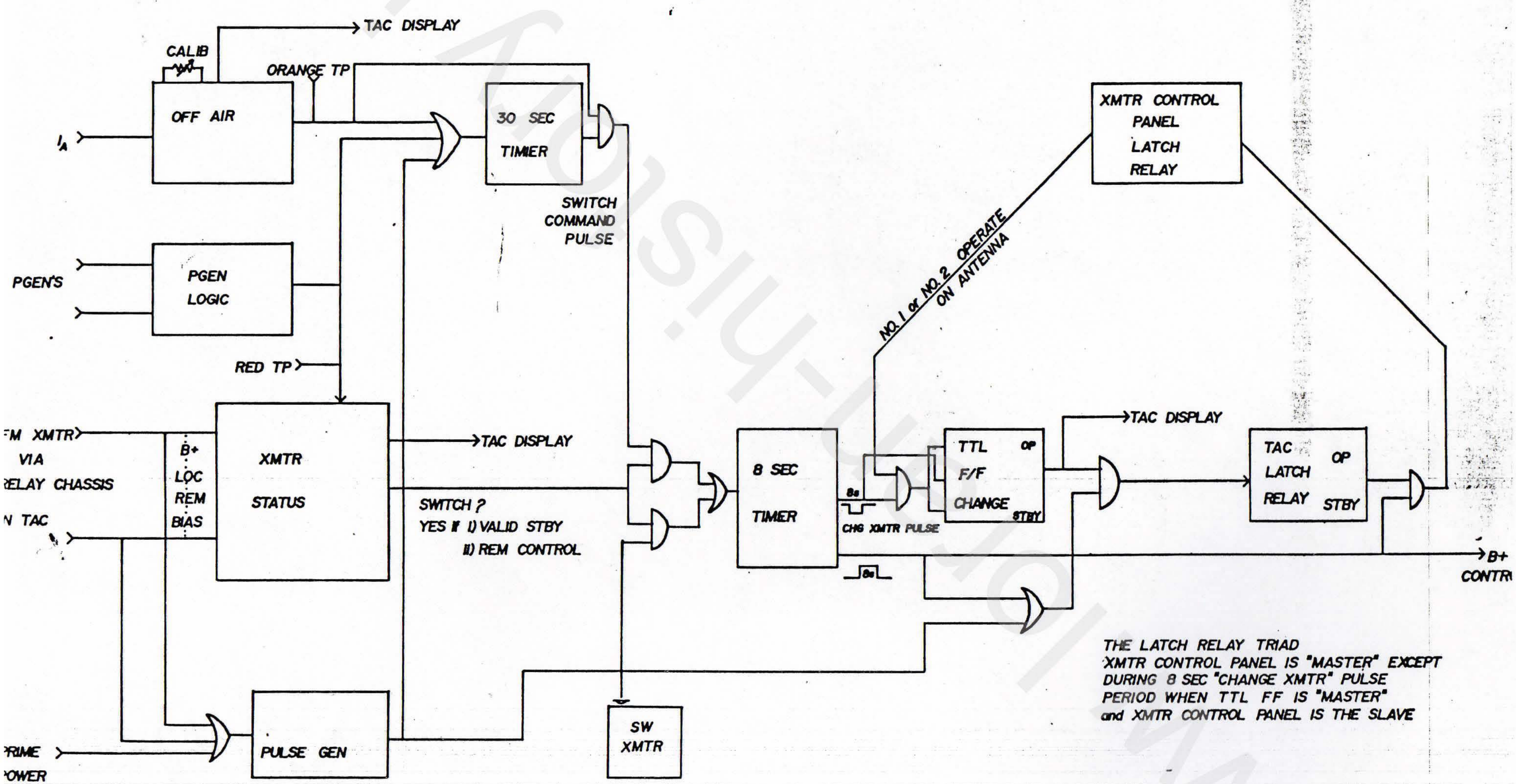


FIGURE 4-1

TAC FUNCTIONAL DIAGRAM

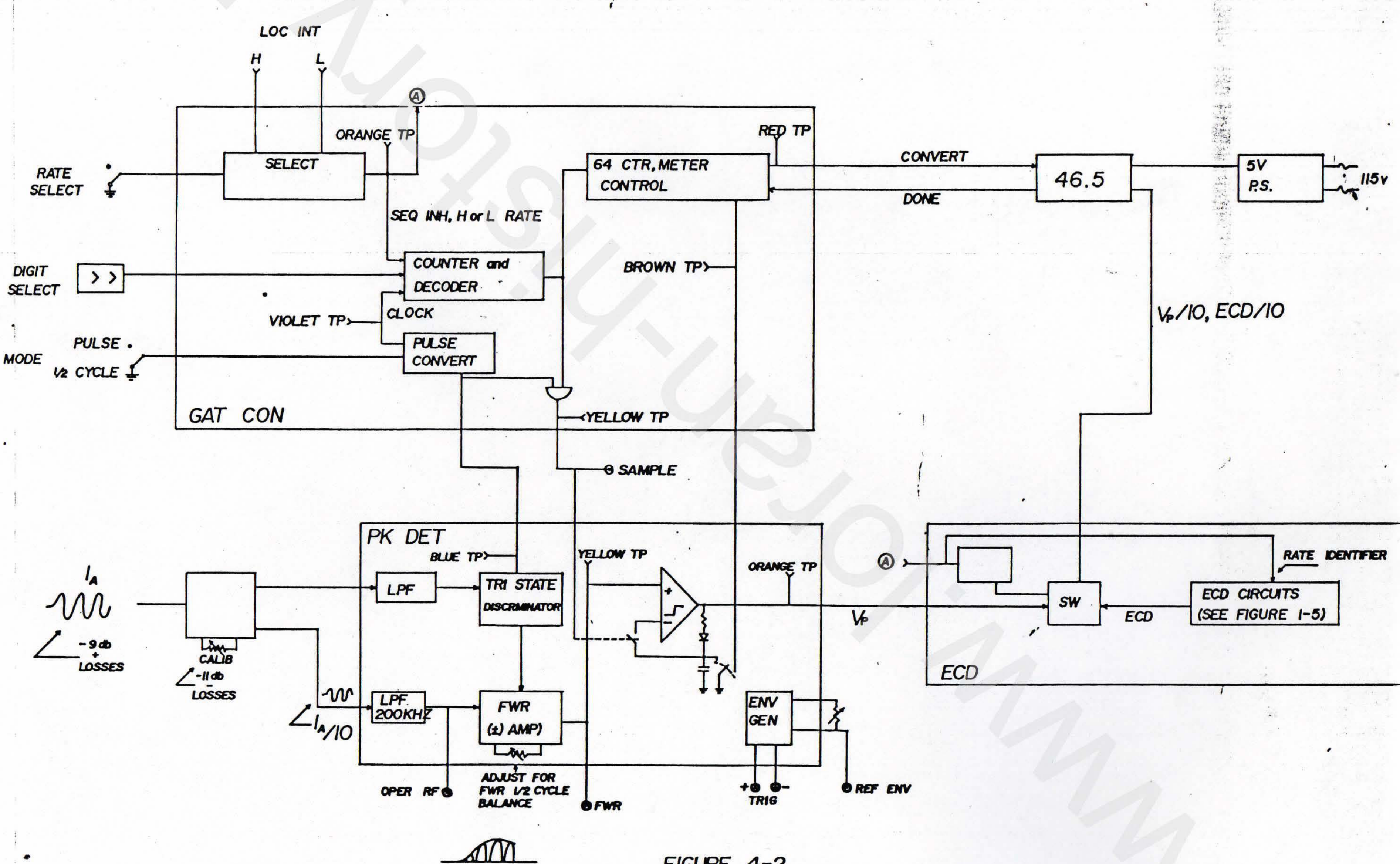


FIGURE 4-2

ELECTRICAL PULSE ANALYZER FUNCTIONAL DIGRAM

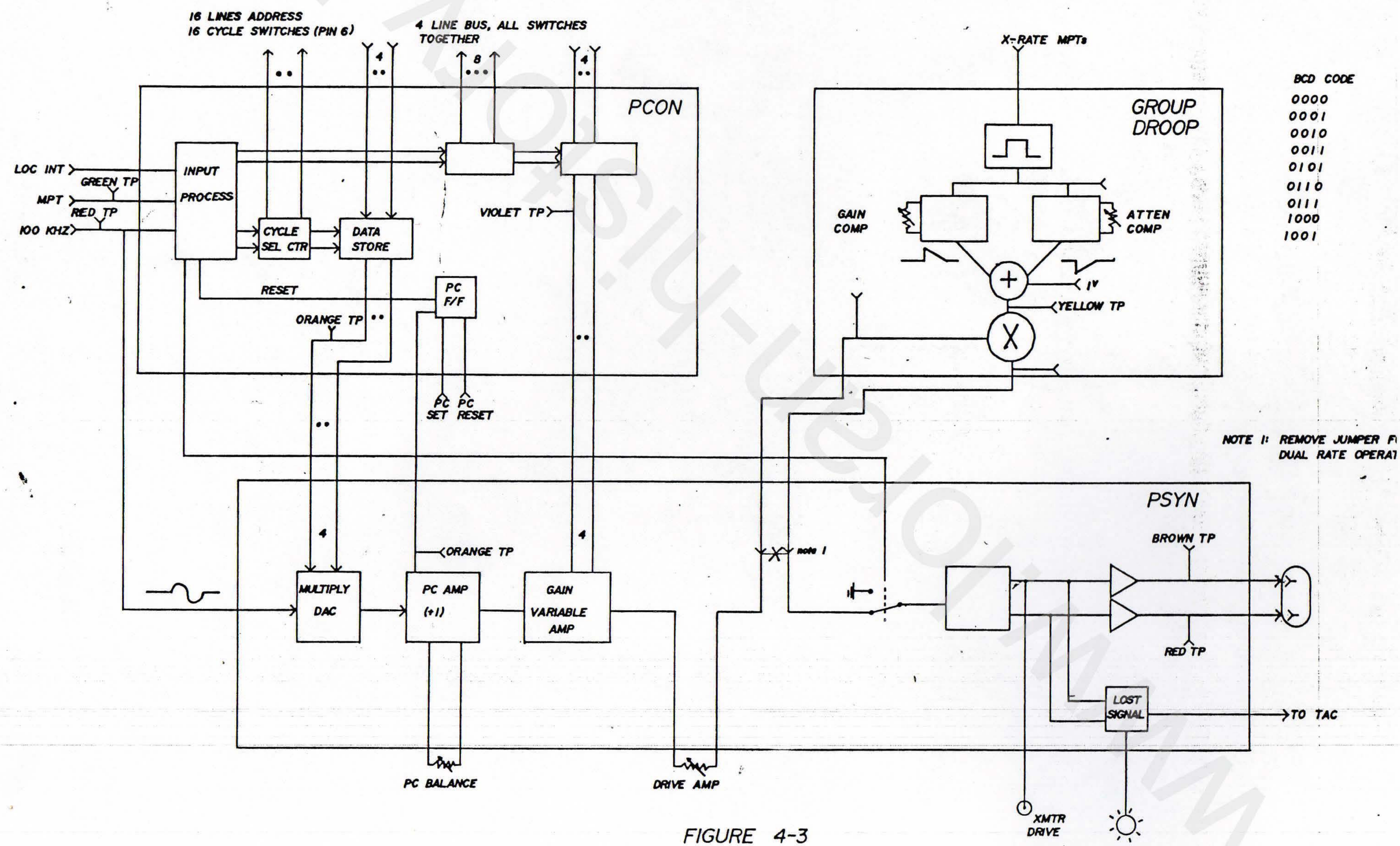

16 LINES ADDRESS
16 CYCLE SWITCHES (PIN 6)
4 LINE BUS, ALL SWITCHES TOGETHER
X-RATE MPTs
BCD CODE
0000
0001
0010
0011
0101
0110
0111
1000
1001
PCON
LOC INT
GREEN TP
MPT
RED TP
100 KHZ
INPUT
PROCESS
CYCLE
SEL CTR
DATA
STORE
4
8
VIOLET TP
RESET
ORANGE TP
PC
F/F
PC
SET
PC
RESET
GROUP
DROOP
GAIN
COMP
ATTEN
COMP
1V
YELLOW TP
NOTE 1: REMOVE JUMPER F
DUAL RATE OPERAT
PSYN
BROWN TP
note 1
MULTIPLY
DAC
PC AMP
(+1)
ORANGE TP
GAIN
VARIABLE
AMP
RED TP
LOST
SIGNAL
TO TAC
PC BALANCE
DRIVE AMP
XMTR
DRIVE

FIGURE 4-3

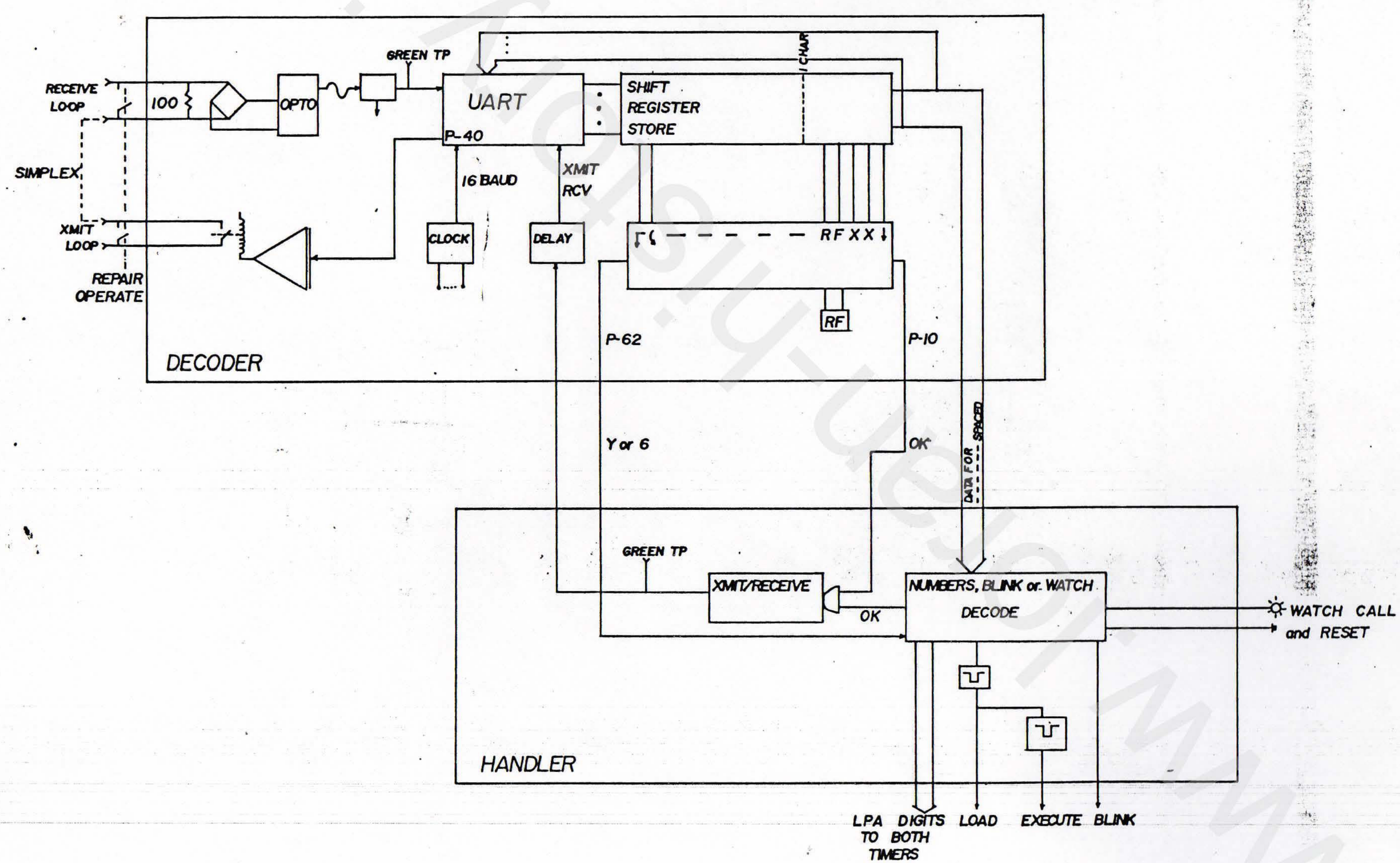

RECEIVE LOOP
100
OPTO
GREEN TP
UART
P-40
16 BAUD
CLOCK
XMIT RCV
DELAY
SHIFT REGISTER STORE
I CHAR
RF X X
RF
SIMPLEX
XMIT LOOP
REPAIR OPERATE
DECODER
P-62
P-10
Y or 6
OK
DATA FOR SPACED
GREEN TP
XMIT/RECEIVE
OK
NUMBERS, BLINK or WATCH DECODE
WATCH CALL and RESET
HANDLER
LPA DIGITS TO BOTH TIMERS
LOAD
EXECUTE
BLINK

FIGURE 4-5

MISCELLANEOUS I/F & SAU FACTS

INTERFACE UNIT: Passive system, splitting signals, isolating them with resistors and combining output signals. Only possible failure items are the xfmrs, combiners, and splitters. Be careful of phasing in any that are changed, get wires correct.

SAU: Major alarms discuesed in parts 1 and particularly 2.

1. The fact that the ECD alarm is inhibited for 2 mins. after a xmtr switch was not made.
2. Be sure you program a new board (see technical manual), many alarms can be disabled!
3. To set the watchdog timer more exactly than given in the manual, clip a 1,2K resistor across R5 (1.2Mohm). The timer will run at 1000 times its normal speed. Set switches for 1/1000 of desired time in minutes.
4. To set your blink and off air counters exactly, blink stby timer and adjust R8 (20K variable) for an accurate total (about 10 minutes).
5. To reduce your lamp consumption, place a zener diode in series with lamp to driver line, 4-6v and adequate current rating.
6. The chart record output can be used if you need a permanent record of alarm events at the station. Four alarms can be recorded on one channel, see the tech. manual.
7. To reduce lamp consumption in the ARU or RAU, replace the 115v types with 220v types of the same base.
8. The spare alarm inputs can be used for both electric alarms and also things such as biulding security, LORAN-A alarms, ETC. Programming this four input alarm is covered in the system manual.

ROUTINE TIMER SWITCH

Several of the watchstander drills require that the timer be witched from operate to standby so that timer no.1 frequency standard path can be interupted without affecting the on air signal. Usually a timer switch is detected at the monitor station as a spike in the ase channel. This is caused by cycle comp having to relock in the new operate timer. This proceedure aligns the cycle comps in the timers so that the amount of error that the new operate timer has to drive is minimal.

STEP 1 : Use a dual trace scope, with two X10 probes, with both channels set to .2 volts/cm and calibrated. Channel "A" polarity should be in normal (or +) and channel "B" polarity should be in invert (or -). The mode setting should be in added.

STEP 2 : Use the red test point of the R card in timer no.1 as channel "A" input and use the red test point of the R card in timer no.2 as channel "B" scope input.

STEP 3 : Put the timers into local control and insert 2 u/sec LPA into the standby timer. This will cause the cycle comp of the standby timer to drive. The waveform on the scope will increase and decrease in amplitude as the cycle comp drives.

STEP 4 : When the signal on the scope reaches its minimum amplitude press the reset to external and insure that the No External Agreement light goes out. This reduces the cycle comp error when switching timers. The timers can now be switched without the monitor or anyone else seeing any change.

NOTE 1 : The standby cycle comp will slowly drive out from this ideal position but it will take a minute or two before the difference becomes great enough to have to relock it.

TIME BASE FAILURE TRAINING SET UP

The purpose of this set up is to teach watchstanders corrective procedures to implement in the event of a dual timer failure and/or an Austron 2000-C failure. The watchstander will learn how to relock the Austron 2000-C receiver, use the TINO number to coarsely resync the TD-989 timer and to use the TINO track to finely resync the TD-989 timer.

THE TEST SET UP

STEP ONE. Using a coax cable long enough to reach from the rear panel of the TIMER CONTROL SET to the rear of the TIC panel, connect one end to the STBY LOCAL INTERVAL at the rear of the TIMER CONTROL SET, the other end to ~~J4~~ J6 of the TIC panel. By using #6 stop on the TIC counter it has a number that is controled by the STBY TMR. This number will be used as the training TINO number.

STEP TWO. Disconnect the OP 1mhz to the Austron 2000-C at the rear of the TIMER CONTROL SET and connect it to the STBY 1mhz jack. This will feed the STBY 1mhz to the phase comparator of the Austron 2000-C so that the TINO track will also be controlled by the STBY TMR.

WATCHSTANDER TRAINING

The " TIME BASE FAILURE " and " AUSTRON LOST-LOCK " Setup will enable the watchstander to relock the Austron and Resync the the timers. The training set up can be simulated by interrupting the frequency standard input to the Austron, thereby causing the reciever to lose lock. The time base failure is simulated by inserting a large, unknown LPA into the standby timer. These simulated tests, properly coordinated with the supervised training set-up as previously described, will allow the watchstander to practice casualty corrective actions, thereby improving their attitude and confidence, in addition to eliminating the fear of the unknown failure.

STEP ONE. Set scope to 1 millisecond per centimeter and ensure that it is in cal. position.

STEP TWO. Check the triggering. There should be a spot where no noise is present on the 9th division from the left (see photo #1). If not present check switch positions. If switch positions are correct turn trigger level knob all the way clockwise and turn back until trace appears. The triggering should now be correct.

STEP THREE. Open right side of Austron reciever and set rate switch to 6. Slew reciever until Master appears. Set rate switch to 5 and position M so it appears as in photo #1.

STEP FOUR. Set scope to 20usec/cm. If pulse appears as in photo #2 it is out of phase code and must be slewed around again. It should appear as in photo #3.

STEP FIVE. Set rate switch to 3. Slew Master so that it appears in photo #3 with the second cycle peak on the first intensified spot. The reciever is now very close to being locked on. Set servo bandwidth to 10 this will help the rcvr lock on quicker. The off light should extinquish.

STEP SIX. While waiting for the reciever to lock on, the TINO number can be used to get the timer close to its proper place in time.

STEP SEVEN. If the Master Amp track is returned to normal you have locked on the correct cycle crossing. If the track is two or more divisions to the right from the originals the Austron has locked on at least 10 usec too high and the reciever must be slewed negative.

STEP EIGHT. With the Austron locked on with M Amp back to original tracks the TINO number and TINO track can be used to bring the timer back in tolerance.

1 MILLISEC/CM 100 MILLIVOLTS

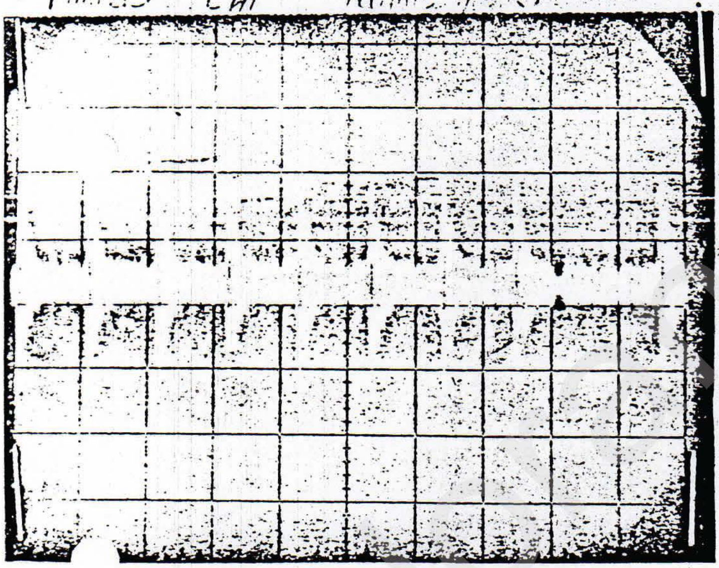


PHOTO #1

20 MICROSECS/CM 100 MILLIVOLTS

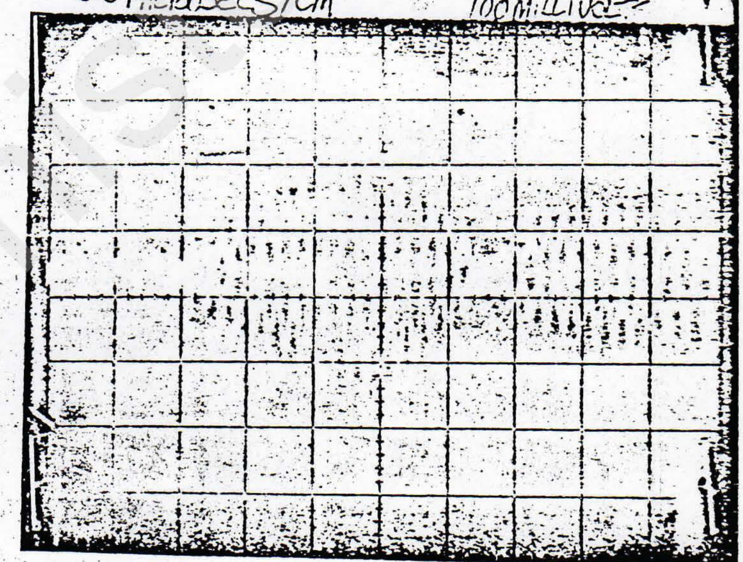


PHOTO #2

20 MICROSECS/CM 100 MILLIVOLTS

PHOTO #3

THE OPERATE OSC Ø ERROR

The purpose of this drill is to teach the watchstander what happens when the Operate Osc experencies a rapid drift type of failure and to train the duty electronics personnel in how to switch Osc 3 into the operate position.

STEP 1 : Do the routine timer switch.

STEP 2 : Change the 1 mhz cable to the Austron 2000-C at the rear of the TCS from the oper 1mhz position to the standby position. This will make the TINO track run from timer no.1 and that will simulate what will happen if timer no.1 were still operate.

STEP 3 : Load a .2 nanosec into the phase microsteppec. This will cause the 5mhz for timer no.1 to change in frequency slightly making it appear the operate cesuim has started to drift rapidly. This will cause the following effects

1. Both phase recorder tracks tracks will start drifting rapidly in the same direction.
2. The standby and Osc 3 LED'S on the SAU will light up.
3. The Operate Ø Error alarm on the SAU will light.
4. A small drift in the TINO track should be apparent.
5. The no external agreement lights will come on in the timers.
6. The Operate Osc fail alarm comes on.

STEP 4 : Have the watchstander simulate a timer switch.

STEP 5 : Have the duty tech patch in and sync up Osc 3 into the operate position. The proceedure is as follows:

1. Take the .2 nanosec insertion out of the phase microstepper.
2. Remove the plug between jacks 1 and 2, this removes the operate osc from the phase microstepper.
3. Remove the plug between jacks 21 and 22 this removes osc 3 from the SAU.
4. Use a jumper cable between jack 21 and jack 2, this puts the Osc 3 into the operate position.
5. Align Osc 3 to the standby Osc by using the phase microstepper to electrical slew the Osc 5mhz to match the Standby Osc. To do this put the rate switch to step. Load a 9 nanosec into the phase microstepper. Push the step button. This will cause the phase recorder track to jump 9 nanosecs. Keep stepping the phase microstepper until the standby phase recorder track is back to originals. When it is back to orignals the adv/RTD LED'S should be extinguscehed.
6. Press the reset to external on timer no.1. The no external agreement lights should extingush.
7. Remove the 9 nanosec from the phase microstepper.
8. Put the Step switch to rate position. All alarms should be out on the SAU.

STEP 6 : To return the Operate Osc back to normal ops remove the plug cable between jack 20 and jack 2 in the patch panel and insert the plugs between jack 1 and jack 2 and between jack 20 and jack 21. Follow instructions 5 thru 7 outlined in step 5.

NOTE 1 : Important; Be sure all microstepper switches and thumbwheel settings are returned to original positions. You may now switch timers.

PRIMARY POWER FAILURE AND BATTERY BACKUP TEST

NOTE: This test will be performed only at the CO's direction. Our present UPS-501 and 312D testing program provides ample checks on the proper operation of these backup power supplies.

STEP 1: Go to the rear of the GCF-RWL-1817A Frequency Standard Set and disconnect the designated standby cesium from its AC source. The front panel-mounted red light labeled "BATTERY" should flash on and off indicating the cesium osc is now being powered by its internal battery pack. This battery pack is rated for a maximum of 30 minutes so the test will let it run for 15 minutes, a good check.

STEP 2: While waiting for the 15 mins to run out, temporarily reconnect the green colored DC battery backup power cable from the 312D power supply to the rear panel of the #2 distribution amp. This will prevent the loss of the standby time base and subsequent loss of the Austron timing reciever during the next step of this test.

STEP 3: At the end of the 15 minute test period mentioned in STEP 1, isolate the standby cesium and the #2 distribution amp from UPS-501 Power Supply by connecting their AC power cords, via an extension cord, to timer room wall power. Now if the UPS-501 should fail during subsequent steps of this test, the stan by time base will remain unaffected.

STEP 4: Breifly disconnect the 115v power to the standby timer by depressing the timer 2 front panel AC circuit breacker on the C-8621/FPN Timer Control Set. Reenergize the AC power. This will check for smooth and proper operation of the CDED-312D power supply and internal timer supplies. The timer should not jump or miss a beat from this AC power interuption.

STEP 5: Switch timers using standard non-emergency timer switch procedures.

STEP 6: Power fail the system by disconnecting the AC power from the UPS-501, and also from the top (normally operate) timer. Interuption of AC power

PRIMARY POWER FAILURE AND BATTERY BACKUP TEST (CONT.)

to the top timer is accomplished by depressing the "timer 1" AC power circuit breaker on the front of the TCS. 15 to 20 minutes of this is a good check of the power supplies.

STEP 7: Repower the entire system, verify proper operation.

STEP 8: Disconnect 115vac power from the operate cesium to verify that it switches to its internal battery pack and operates properly.

STEP 9: Switch timers to standard configuration. Reconnect the standby cesium and #2 distribution amp. to UPS-501/Timing Rack Power. Disconnect the dc powerlines from distribution amp. #2 rear panel. END OF DRILL.

STANDBY OSCILLATOR BURBLE SIMULATION

S P 1: To simulate a stby osc glitch, momentarily interrupt the 5Mhz and 1Mhz signal outputs from the stby cesium. This can be accomplished in a number of ways but the easiest one is to pull, then reconnect, the 5Mhz and 1Mhz looping jacks in the stby cesium lines in the GCF-RWL-2173 frequency patch panel. Next rotate the stby phase shifter dial a large random amount. You now have simulated a sudden and unexplained change in the frequency of the output of the stby oscillator.

STEP 2: This step describes the alarms you should now have, as follows: On the SAU you will see OP TMR FAIL, STBY TMR FAIL, STBY OSC FAIL, and appropriate LED lights will be on. When you press the alarm reset, however, the only alarm that won't clear will be the STBY OSC FAIL. The red "OFF" light on the Austron will probably, but not necessarily, be on. Moving over to the recorder indications, "M AMP" will have changed, "ENV INDEX" will be driving, "TINO TRACK" will be invalid. Next, up above on the TIC counter, the "TINO NUMBER" and "SYNC NUMBER" will be wrong. Over on the timers the "NO EXTERNAL AGREEMENT" light will be energized on both timers and most importantly "CHECK TIMING" alarm on stby timer is lit. This is important because the check timing light is saying DO NOT switch to this timer - something has gone wrong.

S ' 3: In an actual failure situation, the next step would be to patch osc#3 in as stby osc and sync it using the phase resolver dial. In this drill you can simulate this step:(You would remove both the osc #3 looping jack connecting J21 & J22, and the stby osc looping jack connecting J11 & J12. Then patch J21 to J12 using the patch cord provided. To switch the 1Mhz simply remove the BNC cable from the 1Mhz output jack at the rear of the failed cesium and connect it to the new stby cesiums rear panel 1Mhz output jack.)

STEP 4: End of drill (return all systems to normal): Rotate stby osc phase resolver until the LED indications are normal. If necessary, reset stby timer to external. Relock Austron timing reciever by slewing to desired numbers.

FINIS

OSC 3 FAILURE DEMONSTRATION

The purpose of this demonstration is to familiarize the trainee with the Osc alarms in the event of OSC 3 failure or removal.

STEP 1 : Rotate osc 3 phase shifter until the adv/rtd SED lights. Rotate the phase shifter until osc 3 phase error alarm lights. These are the two alarms associated with Osc 3. Return Osc 3 phase shifters to original settings.

STEP 2 : Rotate Stby phase shifters to show sequence of alarms; Stby Adv/Rtd lights, Stby phase error, Stby Osc failure and finnally Stby timer failure.

STEP 3 : Remove plug between J21 and J22 in the frequency patch panel. There are no alarms because the SAU is designed to run without Osc 3.

STEP 4 : Rotate Stby phase shifter to show sequence of alarms; Stby Adv/Rtd LED lights then Op Osc phase error and Stby Osc phase error alarms light simultanously. This happens because the SAU with only two Osc for comparison can not tell which Osc has the phase error.

STEP 5 : Return Stby phase shifter to orginal position and replace plug between J21 and J22 in the frequency patch panel.

OPERATE TMR FAILURE DRILL

..EP 1 - Alin Stby Tmr to Operate in the same manner as in non-emergency Timer switch.

EP 2 - Ground the blue test point on the R card Op Timer by connecting a jumper to the black TP on the R card. This grounds the output of the Timer and puts the station off air. This will cause the following alarms to lite: on the timer, "no transmitter drive" will energize. On both P/GENS: No transmitter drive LEDS will lite. On the TAC: Off air alarm and transmitter failure alarms will lite. However, the TAC will not switch transmitters because both P/GENS show no Xmtr drive, hence there is no Stby xmtr to switch to. On the SAU: Operate timer fail alarm.

STEP 3 - In this drill and in the real situation the next step {without delay} is to switch Timers.

EP 4 - Remove the jumper from the R card of the top {now stby} Timer. If proceeding to OP OSC failure drill go to STEP 2 of that drill. Simulate repairing top Timer. Now to restore system to normal configuration align Stby Tmr to Operate using standard non-emergency Tmr switch proceedures. Remember: The top Timer is now the Standby Timer so do not hit reset to external on the bottom {now Operate} Timer. End of Drill.

OPERATE OSCILLATOR FAILURE DRILL

STEP 1 - SW Timers using standard non-emergency timer switch proceedures. Also move 1mhz to Austron from Operate to Stby {rear of Time Control Unit} and run Stby local PCI to TIC panel J4 to obtain false TIC number.

STEP 2 - At the GCF-RWL-2173 Frequency Patch Panel and operate 5mhz looping Jack {between J1 and J2}. This causes the following alarms: on SAU, a "flickering" operate oscillator fail alarm, all LED'S illuminated; on Timers- "no external agreement" lit. The "flickering" Op Osc fail alarm is caused by the Phase micro-stepper's internal 5mhz oscillator which is still feeding the Timer {hence the Xmtr drive, check timing, etc not energized yet} So the tmr still has a 5mhz input-its just not in the right place. IMPORTANT: This is the indication you would get if you had a failure in the Op 5mhz line before the phase micro-stepper so remeber it! If your microstepper or D/A failer the indications are more definite.

STEP 3 - To show this pull the looping Jack just after the microstepper {from J3 to J4}. Now "OP OSC Fail" on solidly, "No xmtr drive" "DRRG'S" and "Check timing" all energized. In either instance the solution is to switch timers EL PRONTO. Note - The Austron Timing Rcvr does not lose lock.

STEP 4 - In an actual failure, the next step would be to patch a new cesium into the operate oscillator path as was done in Op Osc Ø error drill. To end drill; {Restore system to normal Ops} Replace all looping Jacks, follow standard non-emergency Timer switch procedures, bearing in mind which Timer is actually operate.

XMTR FAILURE DRILLS

The purpose of these drills is to familiarize the trainee with the various alarms associated with different types of transmitter failure. These failures can be divided into two catagories. Equipment failure - where there is an alarm sent to the TAC from the affected eouipment, Low Power - where the RF feedback level is to low causing the OFF AIR alarm to come on in the TAC.

A. OP P-GEN FAILURE
1. Inform SAM that you will be switching Xmtr's.
2. Remove power to Op P-GEN
3. OFF AIR alarm and Xmtr failure alarm in TAC goes off. After 30 seconds TAC switches Xmtrs.
4. SAU indicates Xmtr fail/On air and no Stby Xmtr The Stby Xmtr {the one that had its P-GEN unpluged} will noe have its Stby light on.
5. Restore P-GEN power which will clear the TAC Xmtr failure and will restore the Stby light. Clear the SAU of Xmtr fail/On air alarm.

B. STBY P-GEN FAILURE
1. Remove power to Stby P-GEN
2. Stby light on TAC goes out and Xmtr fail comes on. SAU alarms Xmtr fail/ On air and No Stby Xmtr come on.
3. Restore P-GEN power and clear SAU of Xmtr fail/On air alarm.

C. LOW POWER ALARM
1. Inform SAM that you will be switching Xmtrs.
1a Pencil mark drive pot position - note Stby drive level w/scope on TP5.
2. Reduce drive in operate P-GEN until off air light in TAC comes on
3. After 30 seconds TAC switches Xmtr's.
4. TAC has low power alarm.
5. SAU has no alarms as it does not see a Xmtr failure and thinks it has a good Stby Xmtr.
6. The Stby Xmtr must be recycled to clear low power alarm.
7. Return P-GEN drive to original in accordance w/previous pencil mark and TP5 scope level.

D. OP XMTR FAIL DURING MAINT.
1. Put Xmtrs in local control.
2. Reomve RF feedback cable to TAC {from Ant coupler}.
3. After 1.1 minutes the Xmtr fail/Off air alarm on SAU will turn on

RCI FAILURE

This is potentially the most dangerous failure that can occur. .ne RCI is uded to insert remote commands into the timers {blink,LPA'S}. If the RCI fails and inserts a bogus command into the timers there ill be no locally generated alarms. Because of this the watchstander won't be aware of an abnormality until the monitor contacts him. As the watchcall may not be working, the monitor may try by ringing the TTY bells, or telephone, or by master blinking. The watchstander should take local control of the timers and make whatever corrections are needed.